Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

In the Claims

1. (Currently Amended) A switch circuit comprising:

a first circuit portion corresponding to a first input port;

a second circuit portion corresponding to a second input port; and

an output port,

wherein each of the first and second circuit portions include at least one first transistor providing a portion of an isolation channel, at least one second transistor providing a portion of a transmit channel, and at least two third transistors for providing a control bias for selecting either the transmit channel or the isolation channel; and

wherein each third transistor of the first circuit portion is coupled at its base directly to a base of a corresponding third transistor of the second circuit portion, and to a control voltage source.

2. (Original) The switch circuit of claim 1, wherein the circuit is formed as an integrated circuit.

3. (Previously Presented) The switch circuit of claim 1, wherein the at least two third transistors of each of the first and second circuit portions provides a control bias for selecting which of the first and second input ports are coupled to the output port.

4. (Original) The switch circuit of claim 1, wherein the at least one first transistor comprises two transistors and the at least one second transistor comprises two transistors.

5. (Previously Presented) The switch circuit of claim 1, wherein the at least one second transistor comprises three transistors.

6. (Canceled).

7. (Original) The switch circuit of claim 1, wherein respective emitters of the at least one first transistor and the at least one second transistor are coupled to each other.

8. (Previously Presented) The switch circuit of claim 7, wherein the respective emitters of the at least one first transistor and the at least one second transistor are additionally coupled to a collector of a respective third transistor.

9. (Currently Amended) A method for providing isolation between at least two inputs and an output of a switch circuit comprising the steps of:

providing a first channel for each of the at least two inputs including at least one first differential amplifier pair, said first channel providing isolation between the at least two inputs and the output of the switch circuit;

providing a second channel for each of the at least two inputs including at least one second differential amplifier pair, said second channel providing coupling between one of the at least two inputs and the output of the circuit; and

providing a control bias which selects one of the at least two inputs and a respective first channel or second channel, said control bias comprising at least one biasing transistor corresponding to a first input port coupled at its base directly to a base of at least one second biasing transistor corresponding to a second input port.

10. (Withdrawn) A receiver apparatus comprising:

at least one antenna; and

at least one switch coupled to the antenna, said switch comprising a first circuit portion corresponding to a first input port, a second circuit portion corresponding to a second input port, and an output port, wherein each of the first and second circuit

portions include at least one first transistor providing a portion of an isolation channel, at least one second transistor providing a portion of a transmit channel, and at least one third transistor for providing a control bias for selecting either the transmit channel or the isolation channel.

11. (Canceled).

12. (New) The switch circuit of claim 1, wherein the circuit is formed as an integrated circuit and the at least two third transistors of each of the first and second circuit portions provides a control bias for selecting which of the first and second input ports are coupled to the output port, and the at least one first transistor comprises two transistors and the at least one second transistor comprises two transistors.

13. (New) The switch circuit of claim 1, wherein the at least one second transistor comprises three transistors, and the respective emitters of the at least one first transistor and three second transistors are coupled to each other.